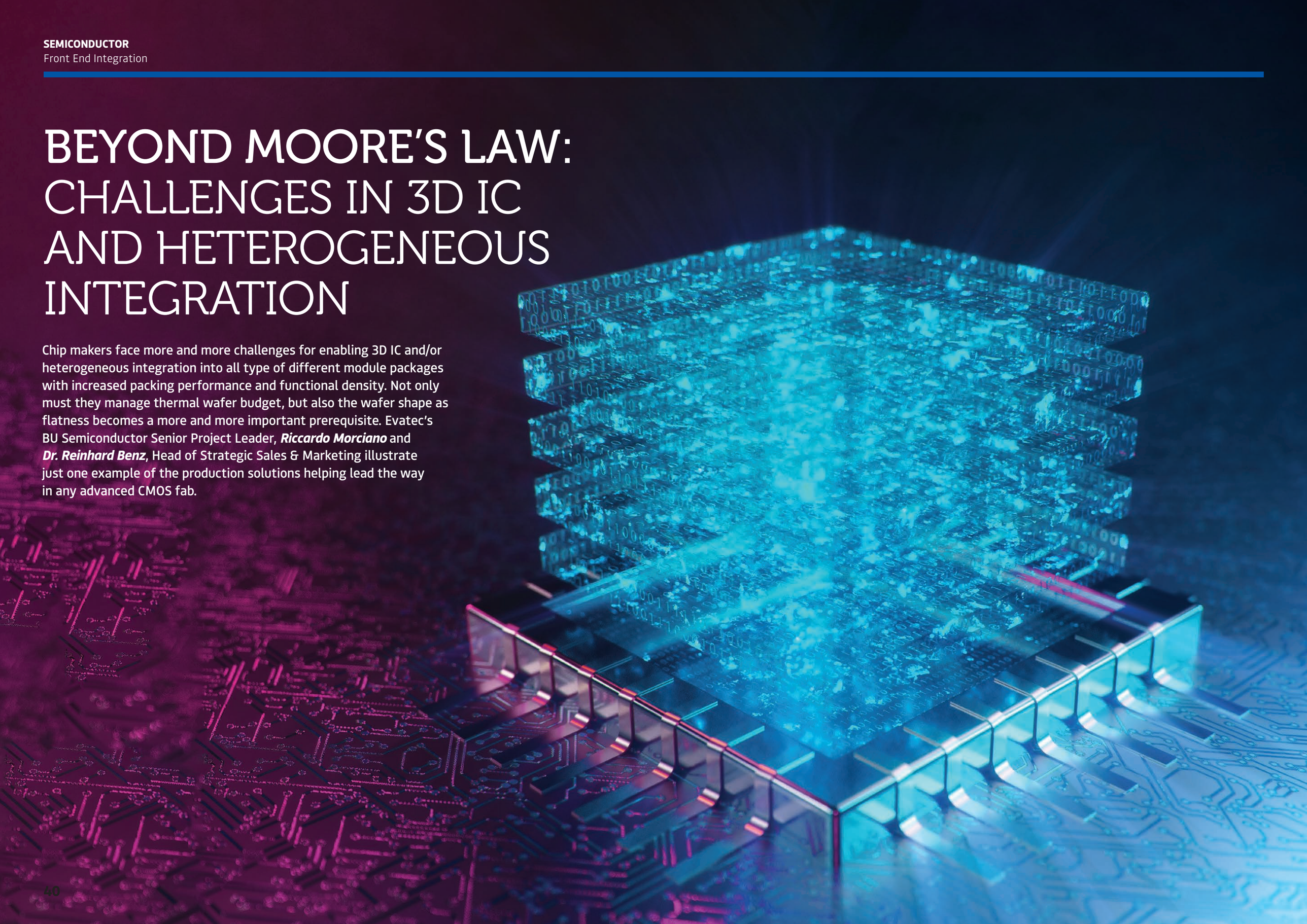
BEYOND MOORE'S LAW: CHALLENGES IN 3D IC AND HETEROGENEOUS INTEGRATION

Chip makers face more and more challenges for enabling 3D IC and/or heterogeneous integration into all type of different module packages with increased packing performance and functional density. Not only must they manage thermal wafer budget, but also the wafer shape as flatness becomes a more and more important prerequisite. Evatec's BU Semiconductor Senior Project Leader, ***Riccardo Morciano*** and ***Dr. Reinhard Benz***, Head of Strategic Sales & Marketing illustrate just one example of the production solutions helping lead the way in any advanced CMOS fab.



Barriers to protect the CMOS backplane might be needed for embedded or the heterogeneous integration of III-V RF- and/or photonic components. Thin film technology can be an ideal solution to address Front End Integration processes such as stress compensation, heat dissipation, diffusion barrier layers and protection layers and therefore master the complexity of 3D IC and hetrogenous integration challenges. Within the latest hard mask technology there's also a need to lower the thermal budget, moving to lower deposition temperatures with sputtering using new oxides or nitride materials.

Solutions for advanced 3D NAND

The increasing number of vertically stacked wafers for increased functional and storage density can lead to wafer deformation and a corresponding substrate warpage. One way to overcome these challenges is backside wafer Warpage Correction (WPC) through a dielectric PVD layer prior to subsequent processing steps (see Figure 1).

Using a compressive nitride PVD solution offers tunable stress films at low temperatures. Key specifications for the desired application which must be fulfilled include stress range, layer thickness, substrate temperature and edge roll-off but also chemical properties for potential post-treatments like the and etch removal process.

Warped wafers can be compensated efficiently using films in the thickness range between a few nanometers and micrometers with a correspondingly high bow correction ratio of about 1µm per nm (Figure 2). If a specific film thickness must be maintained, the film stress or warpage correction can be easily adjusted at constant film thickness.

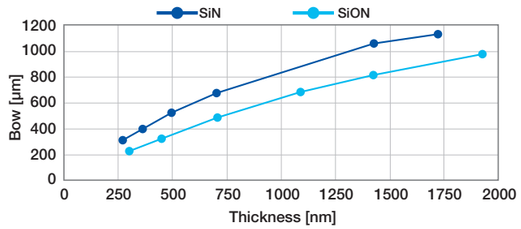


Figure 2: Warpage-thickness ratio

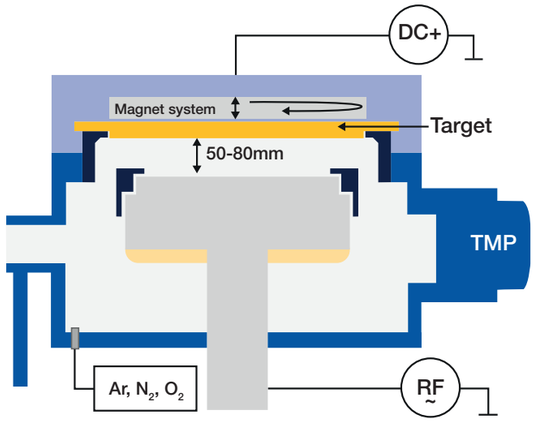


Figure 3: Sputter module configured for nitride film deposition

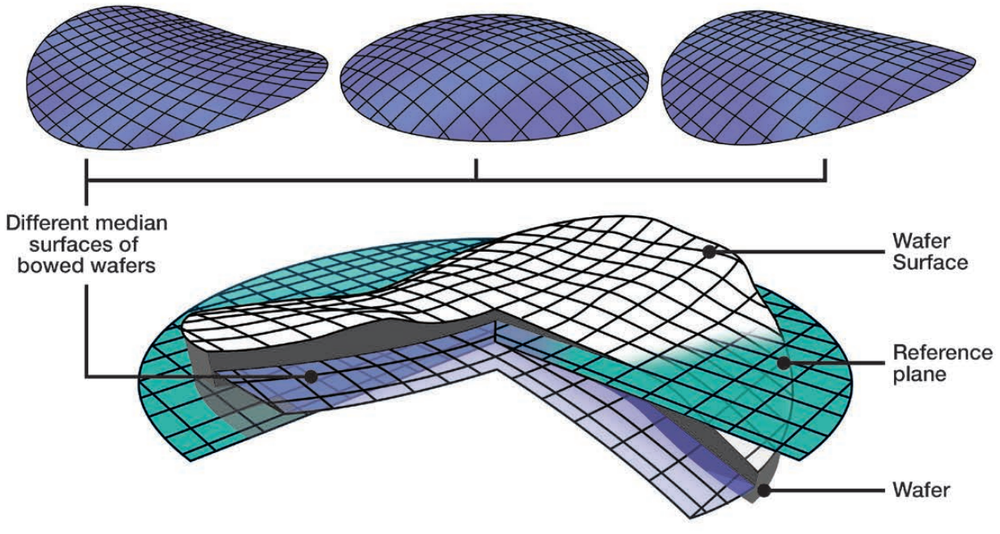


Figure 1: Conceptualising the transition from warped to flat wafers

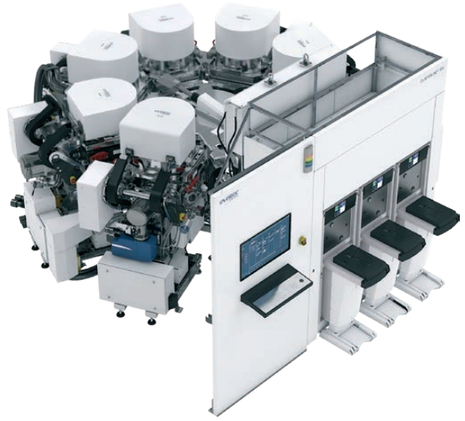


Figure 4: CLUSTERLINE® 300 with up to 6 PVD (DC) modules

CLUSTERLINE® 300 – WPC production solutions are ready

Where the Front End Integration process is part of the BEOL in the CMOS Front End fab, the CLUSTERLINE® 300 platform is available in a dedicated CMOS configuration for improved vacuum, defects and contamination performance.

For the backside Warpage Correction (WPC) application the tool comprises three automatic loadports for 25 wafers (12"), pre-alignment station, flipper and transfer modules included two-arm robot. The sputter modules (with optional shutter) are prepared for nitride film deposition (see Figure 3). A typical tool configuration including 6 DC sputter modules is shown in Figure 4.

Depending on the substrate specification the system can be configured contactless (3mm edge exclusion) and is able to handle warped substrates using dedicated end effectors and shelves. Wafer handling capabilities enable operation with standard Si, thin Si, TAIKO or glass substrates in contamination free <5.0E+10atoms/cm^2 environment and the system has production proven parallel processing scheduling capabilities allowing combination of short and long processes.

To find out more about Evatec's latest generation CLUSTERLINE® 300 platform features visit: **www.evatecnet.com/products/clusterline-family/clusterline-300**

About the authors

Riccardo Morciano
Riccardo has just taken on a new role as Senior Project Leader Development Projects in BU Semiconductor.
His 14 years exeprience in the vacuum and thin film industry at Evatec starting with an apprenticeship, followed by roles incluidng application engineer and project leader stand him in good stead for the challenges ahead.

Dr. Reinhard Benz
Dr. Reinhard Benz joined Evatec in 2013 as Senior Vice President within the Evatec management team. He is Head of Strategic Sales and Product Marketing. He gained a Doctor of Physics degree (Dr.rer.nat) in Applied Physics of Semiconductors from Eberhard-Karls University in Tübingen, Germany and has more than 30 years experience working in the semiconductor and solar capital equipment industries in Europe, Asia and North America.